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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/740,902	12/21/2000	Junichi Asada	201163US2S	6347

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EXAMINER

CHU, CHRIS C

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 09/30/2002

14

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/740,902

Applicant(s)

ASADA, JUNICHI

Examiner

Chris C. Chu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 August 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 28 and 29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 28 and 29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 December 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 28 January 2002 is: a) ☒ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on August 20, 2002 has been received and entered in the case.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the combined limitations in claim 28, lines 18 ~ 23 "wherein the tip portion of said at least the single dummy lead wire covered with said resin molding is positioned between a peripheral portion of said opening portion and a peripheral portion of the semiconductor element arranged within the opening portion, and wherein at least two adjacent dummy lead wires are arranged on said semiconductor device and tip portions of the at least two adjacent dummy lead wires, which have no lead wires therebetween, are connected to each other" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

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3. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 28 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In claim 28, the specification fails to disclose a structure which satisfied the combined limitations “wherein the tip portion of said at least the single dummy lead wire covered with said resin molding is positioned between a peripheral portion of said opening portion and a peripheral portion of the semiconductor element arranged within the opening portion, and wherein at least two adjacent dummy lead wires are arranged on said semiconductor device and tip portions of the at least two adjacent dummy lead wires, which have no lead wires therebetween, are connected to each other.”

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oshino et al. in view of Sugimoto et al.

Oshino et al. discloses in Figs. 1 and 2 a semiconductor memory device comprising:

- a semiconductor element (3);
- a plurality of lead wires (5) connected to a plurality of connecting electrodes (4) formed on said semiconductor element;
- at least a single dummy lead wire (5B) that is not electrically connected to said semiconductor element and does not include an outer lead portion for electrically connecting said semiconductor element to an external circuit of said semiconductor element;
- an insulating film (6) having an opening portion configured to accommodate said semiconductor element and to support said plurality of lead wires connected to the plurality of connecting electrodes of the semiconductor element and said at least the single dummy lead wire; and

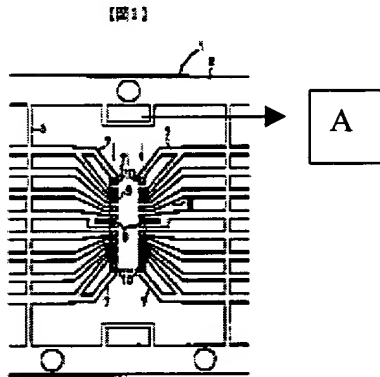
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- a resin molding (7) configured to cover a connecting portion between tip portions of the plurality of lead wires and the plurality of connecting electrodes and a tip portion of said at least the single dummy lead wire within the opening portion of said insulating film,
- wherein said at least a single dummy lead wire (5B, right) is arranged in a space defined by two adjacent lead wires of said plurality of lead wires so that a length of said space is at least twice a minimum pitch between adjacent lead wires of said plurality of lead wires,
- wherein the tip portion of said at least the single dummy lead wire (5B) covered with said resin molding is positioned between a peripheral portion of said opening portion and a peripheral portion of the semiconductor element arranged within the opening portion.
- wherein at least two adjacent dummy lead wires (5B, left) being arranged on said semiconductor device.

Oshino et al. does not disclose tip portions of the at least two adjacent dummy lead wires, which have no lead wires therebetween, being connected to each other. However, Sugimoto et al. discloses in Fig. 1 tip portions of the at least two adjacent dummy lead wires, which have no lead wires therebetween, being connected to each other (see part A in below figure). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Oshino et al. by connecting the two adjacent dummy lead wires as taught by Sugimoto et al. The ordinary artisan would have been motivated to modify Oshino et al. in the manner described above

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for at least the purpose of increasing stably fixing and wire bonding of a semiconductor chip (read problem to be solved, lines 3 and 4).



8. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oshino et al. in view of Candelore.

Oshino et al. discloses in Figs. 1 and 2 a semiconductor memory device comprising:

- a semiconductor element (3);
- a plurality of lead wires (5) connected to a plurality of connecting electrodes (4) formed on said semiconductor element;
- at least a single dummy lead wire (5B) that is not electrically connected to said semiconductor element and does not include an outer lead portion for electrically connecting said semiconductor element to an external circuit of said semiconductor element;
- an insulating film (6) having an opening portion configured to accommodate said semiconductor element and to support said plurality of lead wires

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- connected to the plurality of connecting electrodes of the semiconductor element and said at least the single dummy lead wire; and
- a resin molding (7) configured to cover a connecting portion between tip portions of the plurality of lead wires and the plurality of connecting electrodes and a tip portion of said at least the single dummy lead wire within the opening of said insulating film,
 - wherein said at least a single dummy lead wire (5B, right) is arranged in a space defined by two adjacent lead wires of said plurality of lead wires so that a length of said space is at least twice a minimum pitch between adjacent lead wires of said plurality of lead wires, and
 - wherein a dummy lead wire (5B) is formed on each of two opposing sides of said semiconductor element.

Oshino et al. does not disclose tip portions of the dummy lead wires positioned to face each other being connected to each other to form a straight dummy lead wire.

However, Sugimoto et al. discloses in Fig. 4 tip portions of lead dummy wires (420 and 430) positioned to face each other being connected to each other to form a straight dummy lead wire (421). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Oshino et al. by connecting the two dummy lead wires as taught by Sugimoto et al. The ordinary artisan would have been motivated to modify Oshino et al. in the manner described above for at least the purpose of deterring to probe of the micro-electronic component (column 3, lines 51 and 52).

Response to Arguments

9. Applicant's arguments with respect to claims 28 and 29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

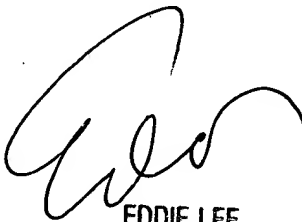
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
September 27, 2002



EDDIE LEE
SUPERVISORY PATENT EXAMINER
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